Abstract

Methods and structure for improving accuracy of a master delay line associated with slave delay lines wherein the master delay line is design utilizing a higher clock frequency then the clock frequency applied to associated slave delay lines, The higher clock frequency applied to the master delay line in accordance with the present invention permits the master delay line to be comprised of fewer delay elements than would be the case for a master delay line using the same basic clock frequency as associated slave delay lines, The lower number of delay elements comprising the master delay line (i.e., the shorter length of the master delay line) helps reduce static phase errors associated with the master delay line inherent in the design, layout and fabrication of a longer delay line.